

**THIN FILM TRANSISTOR ARRAY PANEL AND MANUFACTURING  
METHOD THEREOF**

**BACKGROUND OF THE INVENTION**

5     **(a) Field of the Invention**

          The present invention relates to a thin film transistor array panel and manufacturing method thereof.

**(b) Description of Related Art**

          A thin film transistor (TFT) array panel is utilized for driving pixels of a  
10    display device such as a liquid crystal display (LCD) or an organic electroluminescence  
      (EL) display device. The TFT array panel includes a plurality of gate lines transmitting  
      scanning signals, a plurality of data lines transmitting data signals, a plurality of TFTs  
      connected to the gate lines and the data lines, a plurality of pixel electrode connected to  
      the TFTs, a gate insulating layer covering the gate lines, and a passivation covering the  
15    data lines. The TFT array panel selectively transmits the data signals to the pixel  
      electrodes in response to the scanning signals. The TFT includes a semiconductor layer  
      made of amorphous silicon or polysilicon.

          A conventional method of an amorphous silicon TFT array panel requires  
      several deposition steps and photolithography steps forming the above-described  
20    elements. The increase of the number of the steps reduces the productivity and  
      increases the cost of the products. In addition, the amorphous silicon TFT may be  
      inferior to a polysilicon TFT in operation speed.

## **SUMMARY OF THE INVENTION**

A thin film transistor array panel is provided, which includes: a substrate; a gate electrode; a gate insulating layer formed on the gate electrode; a polysilicon layer formed on the gate insulating layer and including a pair of ohmic contact areas doped with conductive impurity; source and drain electrodes formed on the ohmic contact areas at least in part; a passivation layer formed on the source and the drain electrodes and having a contact hole exposing the drain electrode at least in part; and a pixel electrode formed on the passivation layer and connected to the drain electrode through the contact hole.

The conductive impurity may include boron or phosphorous and the concentration of the impurity may range from about  $1 \times 10^{14}$  to about  $1 \times 10^{16}$ .

The thin film transistor array panel may further include: a gate line disposed between the substrate and the gate insulating layer and connected to the gate electrode; and a data line disposed between the gate insulating layer and the passivation layer and connected to the source electrode.

A method of manufacturing a thin film transistor array panel is provided, which includes: forming a gate electrode; depositing a gate insulating layer and a polysilicon layer on the gate electrode in sequence; forming a photoresist having a first portion and a second portion thinner than the first portion on the polysilicon layer; patterning the polysilicon layer using the photoresist as a mask to form a semiconductor layer; removing the second portion of the photoresist; performing impurity implantation using the first portion of the photoresist as a mask to form ohmic contact areas in the semiconductor layer; removing the first portion of the photoresist; forming source and

drain electrodes on the ohmic contact areas; forming a passivation layer having a contact hole on the drain electrode; and forming a pixel electrode on the passivation layer.

The formation of the photoresist may include: coating a photoresist film on the polysilicon layer; exposing the photoresist film through a photo-mask having a slit  
5 pattern or a translucent portion facing the second portion of the photoresist; and developing the photoresist film to form the photoresist.

The impurity may include p type conductive impurity.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention will become more apparent by describing embodiments  
10 thereof in detail with reference to the accompanying drawings in which:

Fig. 1A is a layout view of a TFT array panel according to an embodiment of the present invention;

Fig. 1B is a sectional view of the TFT array panel shown in Fig. 1A taken along the line IB-IB';

15 Fig. 2A is a layout view of a TFT array panel shown in Figs. 1A and 1B in an initial step of a manufacturing method thereof according to an embodiment of the present invention;

Fig. 2B is a sectional view of the TFT array panel shown in Fig. 2A taken along the line IIB-IIB';

20 Fig. 3 is a sectional view of the TFT array panel shown in Fig. 2A taken along the line IIB-IIB' in a step following the step shown in Fig. 2B;

Fig. 4 is a sectional view of the TFT array panel shown in Fig. 2A taken along the line IIB-IIB' in a step following the step shown in Fig. 3;

Fig. 5A is a layout view of the TFT array panel shown in Figs. 1A and 1B in a step following the step shown in Fig. 4;

Fig. 5B is a sectional view of the TFT array panel shown in Fig. 5A taken along the line VB-VB’;

5 Fig. 6A is a layout view of the TFT array panel shown in Figs. 1A and 1B in a step following the step shown in Figs. 5A and 5B;

Fig. 6B is a sectional view of the TFT array panel shown in Fig. 6A taken along the line VIB-VIB’;

10 Fig. 7A is a layout view of the TFT array panel shown in Figs. 1A and 1B in a step following the step shown in Figs. 6A and 6B;

Fig. 7B is a sectional view of the TFT array panel shown in Fig. 6A taken along the line VIIB-VIIB’;

Fig. 8A is a layout view of the TFT array panel shown in Figs. 1A and 1B in a step following the step shown in Figs. 7A and 7B; and

15 Fig. 8B is a sectional view of the TFT array panel shown in Fig. 8A taken along the line VIIIB-VIIIB’.

### **DETAILED DESCRIPTION OF EMBODIMENTS**

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are  
20 shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

In the drawings, the thickness of layers, films and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that

when an element such as a layer, film, region or substrate is referred to as being “on” another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” another element, there are no intervening elements present.

5           Now, thin film transistor arrays according to embodiments of the present invention will be described with reference to the accompanying drawings.

A TFT array panel according to an embodiment of the present invention is described in detail with reference to Figs. 1A and 1B.

Fig. 1A is a layout view of a TFT array panel according to an embodiment of  
10 the present invention and Fig. 1B is a sectional view of the TFT array panel shown in Fig. 1A taken along the line IB-IB'.

A plurality of gate lines 121 for transmitting gate signals and a gate shorting bar 124 extending substantially in a longitudinal direction are formed on an insulating substrate 110. Each gate line 121 extends substantially in a transverse direction and a  
15 plurality of portions of each gate line 121 form a plurality of gate electrodes 123. Each gate line 121 includes a plurality of projections protruding downward and it may have an expansion having wider width for contact with another layer or an external device.

The gate lines 121 is preferably made of Al containing metal such as Al and Al alloy, Ag containing metal such as Ag and Ag alloy, Cu containing metal such as Cu and  
20 Cu alloy, Cr, Mo, Mo alloy, Ta and Ti. The gate lines 121 may include two films having different physical characteristics, a lower film and an upper film. The upper film is preferably made of low resistivity metal including Al containing metal such as Al and Al alloy for reducing signal delay or voltage drop in the gate lines 121. On the other

hand, the lower film is preferably made of material such as Cr, Mo, Mo alloy, Ta and Ti, which has good physical, chemical, and electrical contact characteristics with other materials such as indium tin oxide (ITO) and indium zinc oxide (IZO). A good exemplary combination of the lower film material and the upper film material is Cr and  
5 Al-Nd alloy.

In addition, the lateral sides of the gate lines 121 are tapered, and the inclination angle of the lateral sides with respect to a surface of the substrate 110 ranges about 30-80 degrees.

A gate insulating layer 140 preferably made of silicon nitride (SiN<sub>x</sub>) is formed  
10 on the gate lines 121.

A plurality of semiconductor islands 154 preferably made of polysilicon are formed on the gate insulating layer 140 opposite the gate electrodes 123. Each semiconductor island 151 includes a pair of ohmic contact areas 163 and 165 doped with n type or p type impurity such as boron (B) and phosphorous P at the top surfaces and are  
15 separated from each other.

The lateral sides of the semiconductor islands 154 are tapered, and the inclination angles thereof are preferably in a range between about 30-80 degrees.

A plurality of data lines 171, a plurality of drain electrodes 175, and a plurality of storage capacitor conductors 177 are formed on the ohmic contacts 161 and 165 and  
20 the gate insulating layer 140.

The data lines 171 for transmitting data voltages extend substantially in the longitudinal direction and intersect the gate lines 121. Each data line 171 may include an expansion having wider width for contact with another layer or an external device.

A plurality of branches of each data line 171, which project toward the drain electrodes 175, form a plurality of source electrodes 173. Each pair of the source electrodes 173 and the drain electrodes 175 are separated from each other and opposite each other with respect to a gate electrode 123. A gate electrode 123, a source electrode 173, and a drain electrode 175 along with a semiconductor island 154 form a TFT having a channel formed in the semiconductor island 154 disposed between the source electrode 173 and the drain electrode 175.

The storage capacitor conductors 177 overlap the projections of the gate lines 121.

The data lines 171, the drain electrodes 175, and the storage capacitor conductors 177 are preferably made of refractory metal such as Mo, Mo alloy or Cr. However, they may further include an additional film located thereon and preferably made of Al containing metal or Ag containing metal.

Like the gate lines 121, the data lines 171, the drain electrodes 175, and the storage capacitor conductors 177 have tapered lateral sides, and the inclination angles thereof range about 30-80 degrees.

The ohmic contact areas 163 and 165 reduce the contact resistance between the underlying semiconductor islands 151 and the overlying data lines 171 and the overlying drain electrodes 175. The semiconductor stripes 151 include a plurality of exposed portions, which are not covered with the data lines 171 and the drain electrodes 175, such as portions located between the source electrodes 173 and the drain electrodes 175.

A passivation layer 180 is formed on the data lines 171, the drain electrodes 175, the storage conductors 177, and the exposed portions of the semiconductor islands

154. The passivation layer 180 is preferably made of photosensitive organic material having a good flatness characteristic, low dielectric insulating material having dielectric constant lower than 4.0 such as a-Si:C:O and a-Si:O:F formed by plasma enhanced chemical vapor deposition (PECVD), or inorganic material such as silicon nitride.

5           The passivation layer 180 has a plurality of contact holes 181 and 182 exposing the drain electrodes 175 and the storage conductors 177. The passivation layer 180 may further has a plurality of contact holes (not shown) exposing the expansions of the data lines 171. The passivation layer 180 and the gate insulating layer 140 may have a plurality of contact holes (not shown) exposing the expansions of the gate lines 121.

10           A plurality of pixel electrodes 191 and, preferably, a plurality of contact assistants (not shown), which are preferably made of ITO or IZO, are formed on the passivation layer 180.

          The pixel electrodes 190 are physically and electrically connected to the drain electrodes 175 through the contact holes 181 and to the storage capacitor conductors 177  
15 through the contact holes 182 such that the pixel electrodes 190 receive the data voltages from the drain electrodes 175 and transmit the received data voltages to the storage capacitor conductors 177.

          The pixel electrodes 190 supplied with the data voltages generate electric fields in cooperation with a common electrode (not shown) on another panel (not shown),  
20 which reorient liquid crystal molecules in a liquid crystal layer (not shown) disposed therebetween.

          A pixel electrode 190 and a common electrode form a liquid crystal capacitor, which stores applied voltages after turn-off of the TFT. An additional capacitor called a



“storage capacitor,” which is connected in parallel to the liquid crystal capacitor, is provided for enhancing the voltage storing capacity. The storage capacitors are implemented by overlapping the pixel electrodes 190 with the gate lines 121 adjacent thereto (called “previous gate lines”). The capacitances of the storage capacitors, i.e.,  
5 the storage capacitances are increased by providing the projections at the gate lines 121 for increasing overlapping areas and by providing the storage capacitor conductors 177, which are connected to the pixel electrodes 190 and overlap the projections, under the pixel electrodes 190 for decreasing the distance between the terminals.

The pixel electrodes 190 overlap the gate lines 121 and the data lines 171 to  
10 increase aperture ratio but it is optional.

The contact assistants are connected to the exposed expansions of the gate lines 121 and the exposed expansions of the data lines 171 through the contact holes. The contact assistants protect the exposed portions and complement the adhesiveness of the exposed portions and external devices.

15 A method of manufacturing the TFT array panel shown in Figs. 1-4 according to an embodiment of the present invention will be now described in detail with reference to Figs. 2A to 8B as well as Figs. 1A and 1B.

Figs. 2A, 5A, 6A, 7A and 8A are layout views of the TFT array panel shown in Figs. 1A and 1B in intermediate steps of a manufacturing method thereof according to an  
20 embodiment of the present invention, and Figs. 2B, 5B, 6B, 7B and 8B are sectional views of the TFT array panel shown in Figs. 2A, 5A, 6A, 7A and 8A taken along the lines IIB-IIB', VB-VB', VIB-VIB', VIIB-VIIB', and VIIIB-VIIIB', respectively.

Referring to Figs. 2A and 2B, a (plurality of) conductive film(s) preferably made of Al, Cr or Mo is sputtered on an insulating substrate 110 such as transparent glass. The conductive film is patterned to form a plurality of gate lines 121 including a plurality of gate electrodes 123. Inclined lateral surfaces of the gate lines 121 facilitate the attachment of following films to the gate lines 121.

Referring to Fig. 3, a gate insulating layer 140 is sequentially deposited on the gate lines 121 and the substrate 110. The gate insulating layer 140 is preferably made of silicon dioxide ( $\text{SiO}_2$ ) or silicon nitride ( $\text{SiN}_x$ ).

Next, an amorphous silicon layer is deposited and heat-treated with laser or furnace to form a polysilicon layer 150. The polysilicon layer 150 may be formed by directly depositing polysilicon.

Referring to Fig. 4, a photoresist film is coated on the polysilicon layer 150 and exposed to a photo-mask and developed to form a photoresist PR having position dependent thickness. The photoresist PR shown in Fig. 4 includes a plurality of first and second portions with decreased thickness. The first portions are located on channel areas B and the second portions are located on contact areas A are indicated.

The position-dependent thickness of the photoresist is obtained by several techniques, for example, by providing translucent areas on the exposure mask 300 as well as transparent areas and light blocking opaque areas. The translucent areas may have a slit pattern, a lattice pattern, a thin film(s) with intermediate transmittance or intermediate thickness. When using a slit pattern, it is preferable that the width of the slits or the distance between the slits is smaller than the resolution of a light exposer used for the photolithography. Another example is to use reflowable photoresist. In detail, once a

photoresist pattern made of a reflowable material is formed by using a normal exposure mask only with transparent areas and opaque areas, it is subject to reflow process to flow onto areas without the photoresist, thereby forming thin portions.

Referring to Figs. 5A and 5B, the polysilicon layer 150 is patterned by using  
5 the photoresist PR as an etch mask to form a plurality of semiconductor islands 150A. The second portions of the photoresist PR on the contact areas A are removed by ashing. At this time, the thickness of the first portions of the photoresist PR may be decreased.

Referring to Figs. 6A and 6B, a plurality of ohmic contact areas 163 and 165  
are formed by implanting impurity into exposed portions of the polysilicon layer 150A  
10 using the first portions of the photoresist PR as an implant mask. The concentration of the impurity is preferably equal to about  $1 \times 10^{14}$  to about  $1 \times 10^{16}$ .

Referring to Figs. 7A and 7B, after the first portions of the photoresist PR are removed, a (plurality of) conductive film(s) preferably made of Al, Cr or Mo is sputtered and patterned to form a plurality of data lines 171 including a plurality of source  
15 electrodes 173, a plurality of drain electrodes, and a plurality of storage capacitor conductors 177.

Referring to Figs. 8A and 8B, a passivation layer 180 preferably made of inorganic material such as silicon nitride or low dielectric organic insulating material is deposited and patterned along with the gate insulating layer 140 to form a plurality of  
20 contact holes 181 and 182. The passivation layer 180 may include two or more films.

Finally, as shown in Figs. 1A and 1B, a plurality of pixel electrodes 190 and a plurality of contact assistants (not shown) are formed on the passivation layer 180 by sputtering and photo-etching an ITO or IZO layer.

The polysilicon channel layer improves characteristics of the TFTs and the use of the photoresist having a position dependent thickness simplifies the manufacturing process.

While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.